Remarks

Claims 1-54 are pending. Claim 13 has been amended to revise its dependency.

The Specification has been amended to update the reference to related applications and to add brief descriptions of Figures 12 and 13. Support for the amendment can be found, for example, on pages 34 and 37 of the specification. No new matter has been added.

The Abstract has been amended to address the Examiner's concerns.

Appreciation is expressed for the indication of allowance of claims 28-35, and allowability of claims 2-4, 9, 11, 13, 16-19, 21-27, 37, 39, 43-45, 49, 52, and 54. However, at this time the applicant chooses to defer amendment of these claims until he has had the opportunity to traverse the Examiner's rejections.

Rejection of Claims under 35 U.S.C. § 102

Claims 1, 6, 13, 36, and 40 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Chen, U.S. Patent No. 6,571,368. The applicant respectfully traverses this rejection.

Chen neither teaches nor suggests a method comprising:

> generating an error polynomial from the data signal using one or more Galois field multiply accumulators each of which contains a Galois field multiplier feeding a Galois field adder;

as required by independent claim 1 and generally required by independent claim 36.

Regarding this operation, the Examiner refers to Chen's Figure 24 and column 17, lines 36-46 which state:

> FIGS. **24** and **25** depict how outputs of the lowest order cells in each of the three sub arrays are combined to generate the error location and error evaluator polynomials. In FIG. **24**, the inputs to Galois Field multiplier **2401** are the output from the lowest order Λodd cell and the factor value at which Λodd is evaluated. The output of multiplier 2401 is combined with output from the lowest order Λeven cell by Galois Field adder **2402**. This output is an evaluation of the error location polynomial at a particular location. When this output is "0", the error value for this position is calculated by Galois Field divider **2501** as depicted in FIG. **25**.

The applicant respectfully submits that the cited use of Galois field adders and multipliers is not for "generating an error polynomial" as required by claim 1, but is instead for evaluating those polynomials. The cited portion of Chen is facially inconsistent. The first sentence states that "FIGS. **24** and **25** depict how outputs . . . are combined to generate the error location and error evaluator polynomials." However, the remaining sentences describe (with reference to the figures) evaluation of the error location polynomial $\Lambda(x)$. To resolve this inconsistency, we refer to other portions of Chen which make clear that Figures 24 and 25 illustrate error polynomial evaluation, not generation.

Chen outlines two distinct steps in column 6, lines 50-65. Those steps are: (1) solving the key equation to obtain the error location polynomial $\Lambda(x)$ and the error evaluation polynomial $\Omega(x)$; and (2) evaluating $\Lambda(x)$ and $\Omega(x)$ to get the error locations and values. For the first step, Chen teaches the use of Euclid's algorithm. For example, column 7, lines 1-8 state:

> The most difficult and computationally complex of these steps is solving the key equation. It is the core of the decoding process. Application of Euclid's algorithm is one of numerous ways to solve the key equation in this step.
>
> Euclid's algorithm is a recursive process of finding the greatest common divisor among x^{2t} and S(x) to solve for $\Lambda(x)$ and $\Omega(x)$. Its stages are initialization, iteration and termination.

Additionally, Figure 5 makes clear that the disclosed process separates out the generation of the error polynomials and the evaluation of the error polynomials. For example, column 8, lines 53-59 state:

> The output of the syndrome computation **511** is a syndrome polynomial S(x), preferably transferred by a parallel output into the Euclid's algorithm logic **512**. The output of the Euclid's algorithm logic **512** is two polynomials, the error location polynomial $\Lambda(x)$, which is passed to evaluator. [sic] **513** and the error evaluator polynomial $\Omega(x)$, which is passed to evaluator **514**.

Chen's Brief Description of the Figures (column 4-5) makes clear that Figures 9-18 depict various aspects of error polynomial generation (i.e., implementation and control

of Euclid's algorithm), while Figures 19-26 depict various aspects of error polynomial evaluation. More specifically, column 5, lines 5-7 states:

> FIGS. **22** and **23** are logic diagrams for Ω and Λ cells in the error evaluator array architecture which embodies the principles of the present invention.
>
> FIGS. **24** and **25** are logic diagrams for combining results from first cell(0), second cell(1) and second cell(0) to determine whether an error is located at a particular term of the message and, if so, the value of the error.

Additionally, the description of Figures 22-25 (e.g., column 17, lines 13-46) taken in conjunction with Chen's systolic array structure for performing calculations (i.e., Figure 6 and column 9, lines 1-43) make clear that Figures 24 and 25 describe operations that occur during the course of evaluating error polynomials, not generating error polynomials as claimed.

Accordingly, the applicant respectfully submit that independent claims 1 and 36 are allowable over Chen. Claims 2-13 depend from claim 1 and are allowable for at least this reason. Claims 37-45 depend from claim 36 and are allowable for at least this reason.

Rejection of Claims under 35 U.S.C. § 103

Claims 5, 7, 8, 10, 14, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Cameron, U.S. Patent No. 6,684,364. Claims 20 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Cameron, and further in view of Weng, U.S. Patent No. 5,710,782. Claims 46, 47, 50, 51, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Theodoras, II et al., U.S. Patent No. 6,751,743 (Theodoras). Claim 48 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Theodoras, and further in view of Weng. The applicant respectfully traverses these rejections.

Regarding independent claim 14, Chen and Cameron, taken alone or in combination, neither teach nor suggest a method including:

> feeding the syndromes to a plurality of Galois field multiply accumulators;
>
> calculating a plurality of minimum-degree polynomials associated with the BCH code, using the Galois field multiply accumulators; and

generating an error polynomial based on the minimum-degree polynomials,

as required by independent claim 14. As above, the Examiner refers to Chen as teaching the claimed error polynomial calculation using Galois field multiply accumulators. The applicant respectfully submits for that for the same reasons as outline above, Chen neither teaches nor suggests using Galois field multiply accumulators as part of error polynomial calculation. Accordingly, the applicant respectfully submits that independent claim 14 is allowable over Chen and Cameron. Claims 15-27 depend from claim 14 and are allowable for at least this reason.

Regarding independent claim 46, the applicant notes that since the present application was filed on or after November 29, 1999, changes made to 35 U.S.C. §103(c) by the American Inventors Protection Act of 1999 are applicable to the present case. Accordingly, the applicant states for the record that at the time the present invention was made, it and the subject matter disclosed in Theodoras were owned by the same person or subject to an obligation of assignment to the same person. Accordingly, the applicant respectfully submits that Theodoras is not proper prior art for the purposes of 35 U.S.C. §103 and rejections based on Theodoras should be withdrawn. Accordingly, the applicant respectfully submits that independent claim 46 is allowable over Chen. Claims 47-54 depend from claim 46 and are allowable for at least this reason.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on November 1, 2004.

Attorney for Applicant(s)

11/1/04

Date of Signature

Respectfully submitted,

Marc R. Ascolese
Attorney for Applicant(s)
Reg. No. 42,268
512-439-5085
512-439-5099 (fax)